



SEGA OF AMERICA, INC.
Consumer Products Division

Rex Sabio
242

32X H/W Information

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32X HW Information (1)

General Target Items

April 28, 1994

1. SDRAM (8 bytes read / single write)
 - Read 11 Clock / 8 word
 - Write 2 Clock / 1 word
2. 32X Mode, cartridge access, wait count (R/W common)
 - SH2 6 wait (min.) ~ 15 wait (max.)
 - 68K 0 wait (min.) ~ 5 wait (max.)
3. 68K system register access, wait count (R/W common)
 - 0 wait
4. 68K VDP access, wait count
 - Frame buffer (Read) 2 wait (min.) read, write (max.)
 - Frame buffer (Write) 0 wait
 - Register (Read) 2 wait
 - Register (Write) 0 wait
 - Palette (Read) 2 wait (min.) ~ 64 wait
 - Palette (Write) 3 wait (min.) ~ 64 wait

Note The wait count is a reservation of public CPU operation clock.
1 wait count at 64 wait means this is read of 1 line on the display screen is required.

- a. When 320 dots of pixel data cannot be reserved within the frame buffer, caution must be used because the image data is displayed. (Line table is drawn)



- b. 0 byte cannot be written to the frame buffer but 1 ~ FF can. 0 word write is possible

32X H/W information (2)

Target Ver. 1.0 Items (and differences with Ver. 2.0)

April 28, 1994

1. Target Dip Switches

System Board (TPI-4792)

| | default | | default | | default |
|----------------|---------|----------------|---------|----------------|---------|
| * 1-1 JAVEXT | ON | * 2-1 SH2M-MD0 | OFF | * 3-1 SH2S-MD0 | OFF |
| * 1-2 NTSC/PAL | OFF | * 2-2 SH2M-MD1 | ON | * 3-2 SH2S-MD1 | ON |
| * 1-3 H.C. | OFF | * 2-3 SH2M-MD2 | OFF | * 3-3 SH2S-MD2 | OFF |
| * 1-4 H.C. | OFF | * 2-4 SH2M-MD3 | OFF | * 3-4 SH2S-MD3 | OFF |
| | | * 2-5 SH2M-MD4 | ON | * 3-5 SH2S-MD4 | ON |
| | | * 2-6 SH2M-MD5 | ON | * 3-6 SH2S-MD5 | OFF |
| | | * 2-7 H.C. | OFF | * 3-7 H.C. | OFF |
| | | * 2-8 H.C. | OFF | * 3-8 H.C. | OFF |

VDP H/W Board (TPI-6618)

| | default |
|--------------|---------|
| * 1-1 ROM/IO | ON |
| * 1-2 ROM/IO | ON |
| * 1-3 ROM/IO | ON |
| * 1-4 G.A. | ON |
| * 1-5 H.C. | OFF |
| * 1-6 H.C. | OFF |
| * 1-7 H.C. | OFF |
| * 1-8 H.C. | OFF |

VDP Board (TPI-6618)

| | NTSC (default) | PAL |
|-------|----------------|-----|
| * JP1 | ON | OFF |
| * JP2 | ON | ON |
| * JP3 | ON | ON |

Clock Board (TPI-6408)

| | NTSC/PAL |
|-------|----------|
| * JP1 | ON |
| * JP2 | ON |
| * JP3 | ON |
| * JP4 | OFF |
| * JP5 | OFF |
| | ON |

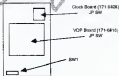
* Change not allowed

- * When PS-A board master is used, set system board DSM2-1 to ON and DSM2-2 to OFF
- * When PS-A board slave is used, set system board DSM2-1 to ON and DSM2-2 to OFF
(May 1st 1994 addition)

Main Board (TPI-4792)



VDP H/W Board (TPI-6618)



2. I2X I/F Implementation Time

| SH-2 Access Destination | Target Ver. 1.0 | Target Ver. 2.0 |
|--------------------------|-----------------|-----------------|
| Boot ROM (ROM) | 3 Clock | 3 Clock |
| System Register (RAM) | 3 Clock | 3 Clock |
| WCF Register (RAM) | 4 Clock (max.) | 7 Clock (max.) |
| Header (RAM) | 4 Clock (max.) | 7 Clock (max.) |
| Frame Buffer (shared) | 2 Clock (max.) | 7 Clock (max.) |
| Frame Buffer (2nd Write) | 2 Clock (max.) | 3 Clock (max.) |
| Frame Buffer (3rd Write) | 2 Clock (max.) | 3 Clock (max.) |
| Frame Buffer (4th Write) | 2 Clock (max.) | 3 Clock (max.) |
| Frame Buffer (5th Write) | 2 Clock (max.) | 3 Clock (max.) |
| Frame Buffer (6th Write) | 7 Clock (max.) | 3 Clock (max.) |
| Frame Buffer (7th Write) | 7 Clock (max.) | 3 Clock (max.) |
| Frame Buffer (8th Write) | 7 Clock (max.) | 3 Clock (max.) |
| System Register (RAM) | 4 Clock | 4 Clock |

- Note:** When access to the SH-2 Frame Buffer assumes a continuous access with no Mdr Cycle. When the Mdr Cycle is inserted between accesses, the Mdr access time is shortened only by the number entered by the Mdr Cycle Register which is shorter than a 3 Clock minimum cycle.
- The boot ROM used for Ver. 1.0 SH-2 can use SDRAM with 4 Mbits. Ver. 2.0 and after use a 4-Mbit SDRAM, but because the SH-2 setting is regarded as 2-Mbit, the setting with ICE should be changed to 4-Mbit. At volume production, 2-Mbit SDRAMs are used. While implementing a 4 Mbit setting during development, please delete the setting program.
 - Displays dot distortion with MD.
Left 1/3 dot for Ver. 1.0, 1/3 dot left or right for Ver. 2.0.
Between 1/3 dot left to 1/3 dot right for mass production goods (undefined by MD version).
 - Difference of brightness with MD.
Ver. 1.0 brightness is slightly different; Ver. 2.0 brightness is identical.
In Ver. 1.x, the pattern could be unstable due to color variation in the draw data border area.
 - Ver. 1.0 cannot read the PWM registers; Ver. 2.0 can.
- May 5, 1994**
- Ver. 1.0 cannot use the CD-ROM I/F; Ver. 2.0 can.
Measures against Ver. 1.x could be taken and released as Ver 1.x CD, but only in special cases. However, these measures are normally not applied.
 - In Ver 1.x, anything other than "JAPAN" is not allowed. (Set DIP SW 171-6797 J-1 to ON.) CD I/F Boot ROM for the US becomes Boot ROM for Japan use. (Ver 1.x only) (May 31, 1994)

9. The following countermeasures should be performed in response to PAL.

• For Target Ver. 1.0

- (1) Dip switch changes of the main board
DIPSW1-2 is on

- (2) Crystal exchange of the main board



- (3) Crystal exchange of the I/F board



- (4) Change in VDP board jumper switch



• For Target Ver. 1.1

- (1) Change the game to be Target Ver. 1.0
(2) Crystal exchange of the I/F board



- (3) Change in VDP board Dip switch
DIPSW1-1 is on

* Board combinations

Ver. 1.0 Main Board (171-6797B), I/F Board (171-6815A), VDP Board (171-6804A)

Ver. 1.1 Main Board (171-6797B), I/F Board (171-6815B), VDP Board (171-6816B)

10. DMA (using FIFO) restrictions from 65535 to 5H2.
Limit the amount of data sent per transfer in Ver. 1.x to under 100h words
Due to the characteristics of the ALTRA chip, constraints per Ver. 1.x are
not possible

This restriction does not apply to Ver 2.0

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32X H/W Information (3)

Items Related to ICE and Peripheral Development Devices

May 5, 1994

1. ICE CPU mode setting
 - 68000 Set to SE if using master per command MDnC; set to SE if using slave
 - EVA board Set short pin 36 to ON if using master; set to OFF if using slave
2. SH2 socket Master/Slave position

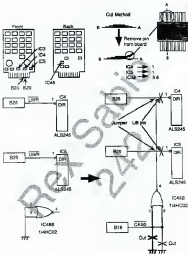


May 27, 1994

1. Precautions when using a 32 Mbit SRAM board
 - The 32 Mbit SRAM W / 68000 board can be used on the SH2 RAM board when both 68000 and SH2 are running.
 - The modifications in the settings are required for 32X development.
 - There are no problems when running 68000 and SH2 independently.
 - There is no need for modifying MD development.



• **Modification Method of the 2016-2017 1099-B Form**



1999, 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021, 2022, 2023, 2024, 2025, 2026, 2027, 2028, 2029, 2030, 2031, 2032, 2033, 2034, 2035, 2036, 2037, 2038, 2039, 2040, 2041, 2042, 2043, 2044, 2045, 2046, 2047, 2048, 2049, 2050, 2051, 2052, 2053, 2054, 2055, 2056, 2057, 2058, 2059, 2060, 2061, 2062, 2063, 2064, 2065, 2066, 2067, 2068, 2069, 2070, 2071, 2072, 2073, 2074, 2075, 2076, 2077, 2078, 2079, 2080, 2081, 2082, 2083, 2084, 2085, 2086, 2087, 2088, 2089, 2090, 2091, 2092, 2093, 2094, 2095, 2096, 2097, 2098, 2099, 2100, 2101, 2102, 2103, 2104, 2105, 2106, 2107, 2108, 2109, 2110, 2111, 2112, 2113, 2114, 2115, 2116, 2117, 2118, 2119, 2120, 2121, 2122, 2123, 2124, 2125, 2126, 2127, 2128, 2129, 2130, 2131, 2132, 2133, 2134, 2135, 2136, 2137, 2138, 2139, 2140, 2141, 2142, 2143, 2144, 2145, 2146, 2147, 2148, 2149, 2150, 2151, 2152, 2153, 2154, 2155, 2156, 2157, 2158, 2159, 2160, 2161, 2162, 2163, 2164, 2165, 2166, 2167, 2168, 2169, 2170, 2171, 2172, 2173, 2174, 2175, 2176, 2177, 2178, 2179, 2180, 2181, 2182, 2183, 2184, 2185, 2186, 2187, 2188, 2189, 2190, 2191, 2192, 2193, 2194, 2195, 2196, 2197, 2198, 2199, 2200, 2201, 2202, 2203, 2204, 2205, 2206, 2207, 2208, 2209, 2210, 2211, 2212, 2213, 2214, 2215, 2216, 2217, 2218, 2219, 2220, 2221, 2222, 2223, 2224, 2225, 2226, 2227, 2228, 2229, 2230, 2231, 2232, 2233, 2234, 2235, 2236, 2237, 2238, 2239, 2240, 2241, 2242, 2243, 2244, 2245, 2246, 2247, 2248, 2249, 2250, 2251, 2252, 2253, 2254, 2255, 2256, 2257, 2258, 2259, 2260, 2261, 2262, 2263, 2264, 2265, 2266, 2267, 2268, 2269, 2270, 2271, 2272, 2273, 2274, 2275, 2276, 2277, 2278, 2279, 2280, 2281, 2282, 2283, 2284, 2285, 2286, 2287, 2288, 2289, 2290, 2291, 2292, 2293, 2294, 2295, 2296, 2297, 2298, 2299, 2300, 2301, 2302, 2303, 2304, 2305, 2306, 2307, 2308, 2309, 2310, 2311, 2312, 2313, 2314, 2315, 2316, 2317, 2318, 2319, 2320, 2321, 2322, 2323, 2324, 2325, 2326, 2327, 2328, 2329, 2330, 2331, 2332, 2333, 2334, 2335, 2336, 2337, 2338, 2339, 2340, 2341, 2342, 2343, 2344, 2345, 2346, 2347, 2348, 2349, 2350, 2351, 2352, 2353, 2354, 2355, 2356, 2357, 2358, 2359, 2360, 2361, 2362, 2363, 2364, 2365, 2366, 2367, 2368, 2369, 2370, 2371, 2372, 2373, 2374, 2375, 2376, 2377, 2378, 2379, 2380, 2381, 2382, 2383, 2384, 2385, 2386, 2387, 2388, 2389, 2390, 2391, 2392, 2393, 2394, 2395, 2396, 2397, 2398, 2399, 2400, 2401, 2402, 2403, 2404, 2405, 2406, 2407, 2408, 2409, 2410, 2411, 2412, 2413, 2414, 2415, 2416, 2417, 2418, 2419, 2420, 2421, 2422, 2423, 2424, 2425, 2426, 2427, 2428, 2429, 2430, 2431, 2432, 2433, 2434, 2435, 2436, 2437, 2438, 2439, 2440, 2441, 2442, 2443, 2444, 2445, 2446, 2447, 2448, 2449, 2450, 2451, 2452, 2453, 2454, 2455, 2456, 2457, 2458, 2459, 2460, 2461, 2462, 2463, 2464, 2465, 2466, 2467, 2468, 2469, 2470, 2471, 2472, 2473, 2474, 2475, 2476, 2477, 2478, 2479, 2480, 2481, 2482, 2483, 2484, 2485, 2486, 2487, 2488, 2489, 2490, 2491, 2492, 2493, 2494, 2495, 2496, 2497, 2498, 2499, 2500, 2501, 2502, 2503, 2504, 2505, 2506, 2507, 2508, 2509, 2510, 2511, 2512, 2513, 2514, 2515, 2516, 2517, 2518, 2519, 2520, 2521, 2522, 2523, 2524, 2525, 2526, 2527, 2528, 2529, 2530, 2531, 2532, 2533, 2534, 2535, 2536, 2537, 2538, 2539, 2540, 2541, 2542, 2543, 2544, 2545, 2546, 2547, 2548, 2549, 2550, 2551, 2552, 2553, 2554, 2555, 2556, 2557, 2558, 2559, 2560, 2561, 2562, 2563, 2564, 2565, 2566, 2567, 2568, 2569, 2570, 2571, 2572, 2573, 2574, 2575, 2576, 2577, 2578, 2579, 2580, 2581, 2582, 2583, 2584, 2585, 2586, 2587, 2588, 2589, 2590, 2591, 2592, 2593, 2594, 2595, 2596, 2597, 2598, 2599, 2600, 2601, 2602, 2603, 2604, 2605, 2606, 2607, 2608, 2609, 2610, 2611, 2612, 2613, 2614, 2615, 2616, 2617, 2618, 2619, 2620, 2621, 2622, 2623, 2624, 2625, 2626, 2627, 2628, 2629, 2630, 2631, 2632, 2633, 2634, 2635, 2636, 2637, 2638, 2639, 2640, 2641, 2642, 2643, 2644, 2645, 2646, 2647, 2648, 2649, 2650, 2651, 2652, 2653, 2654, 2655, 2656, 2657, 2658, 2659, 2660, 2661, 2662, 2663, 2664, 2665, 2666, 2667, 2668, 2669, 2670, 2671, 2672, 2673, 2674, 2675, 2676, 2677, 2678, 2679, 2680, 26

• Modification Method of the 18 Meg SPARC WBUP Board



Work Procedure

1. Lift pin 1 of U31 and U32.
2. Lift pins 13, 14, and 15 of U33.
3. Add jumper between pin 16 of U30 and pins 13 and 14 of U31.
4. Connect pin 15 of U33 to GND (pin 6).
5. Add jumper between pin 9 of U33 and pin 1 of each U31 and U32.

• After Modification

